AMENDMENT TO THE CLAIMS

This listing of claims will replace all prior versions of claims in the application.

Listing of Claims:

1. (currently amended) In an integrated circuit multichannel packet transfer device, an apparatus for transferring a plurality of data packets, comprising:

a first interface circuit for receiving packet data on a first channel;

a memory;

a packet manager circuit coupled between the first interface circuit and the memory to receive data on the first channel from the first interface circuit, wherein the packet manager circuit is configured to write at least a first data packet fragment to the memory under control of a first descriptor, and is configured to write ~~at least a second~~ additional data packet fragments to the memory under control of ~~a second~~ corresponding additional descriptors;

a register for storing a minimum descriptor count;

a timer for generating a first time-out signal at a predetermined time after the first descriptor is ready for transfer; and

a controller for controlling descriptor write back operations to memory in either read-modify-write mode or write-invalidate mode, wherein the controller writes a plurality of descriptors together to memory in a single write-invalidate operation only if the plurality of descriptors that are ready for transfer meets or exceeds the minimum descriptor count and if the plurality of descriptors ~~is~~ that are ready for transfer meets or exceeds the minimum descriptor count before the first time-out signal is generated.

2. (original) The apparatus recited in claim 1, wherein the controller writes the plurality of descriptors separately to memory as a sequence of read-modify-write operations if the plurality of descriptors is not ready for transfer before the first time-out signal is generated.

3. (original) The apparatus recited in claim 1, wherein the timer comprises

a multi-bit counter,

a multiplexer having one select line, one output and multiple inputs, with each input coupled to a corresponding bit of the multi-bit counter,

a timer control register coupled to the select line of the multiplexer, and

a first pulse generator coupled to the multiplexer output for generating the first time-out signals,

wherein the multiplexer selects one of the bits in the multi-bit counter for output to the pulse generator in response to the timer control register to generate the first time-out signal.

4. (currently amended) The apparatus recited in claim 1, where the memory comprises a cache memory having a line width of 2N bytes, and the ~~first and second~~ descriptors each have a width of N bytes, where N is a positive integer.

5. (original) The apparatus recited in claim 1, where the memory comprises a system memory and a cache memory, such that the packet manager writes data packets or descriptors to the system memory or cache memory.

6. (canceled)

7. (original) The apparatus recited in claim 1, where the timer comprises a memory device for programmably storing a timer setting to selectively determine the predetermined time at which the first time-out signal is generated.

8. (currently amended) The apparatus recited in claim 1, comprising:

a second interface circuit for transmitting packet data on a second channel;

an packet manager output circuit coupled between the memory and the second interface circuit to transmit data from the memory on the second channel, wherein the packet manager output circuit is configured to write output data packets to the second interface circuit under control of a plurality of output descriptors;

a second timer for generating a second time-out signal a predetermined time after a first output descriptor of the second channel is ready for transfer; and

a output controller for controlling output descriptor write back operations to memory in either read-modify-write mode or write-invalidate mode, wherein the output controller writes a plurality of output descriptors together to memory in a single write-invalidate operation if the plurality of output descriptors is ready for transfer before the second time-out signal is generated.

9. (original) The apparatus recited in claim 8, wherein the output controller writes the plurality of output descriptors separately to memory as a sequence of read-modify-write operations if the plurality of output descriptors is not ready for transfer before the second time-out signal is generated.

10-16. (canceled)

17. (currently amended) A method comprising:

setting a minimum descriptor count;

setting a first time-out period;

receiving a first packet fragment in an interface circuit;

receiving ~~a second~~ subsequent packet fragments in the interface circuit;

transmitting the first and ~~second~~ subsequent packet fragments from the interface circuit to a memory under control of ~~the first and second~~ corresponding descriptors~~, respectively~~; and

~~setting a timer to expire a predetermined time interval after the first descriptor for the first packet fragment is released; and~~

~~writing the first and second descriptors back to memory together as a write-invalidate command if the second descriptor is released before expiration of the timer~~

performing write back operations to memory in either read-modify-write mode or write-invalidate mode, wherein a plurality of descriptors are written back together in a single write-invalidate operation only if the plurality of descriptors that are ready for transfer meets or exceeds the minimum descriptor count and if the plurality of descriptors that are ready for transfer meets or exceeds the minimum descriptor count before the first time-out period expires.

18. (currently amended) The method recited in claim 17, further comprising writing the first and ~~second~~ subsequent descriptors back to memory separately as a sequence of read-modify-write commands if the ~~second~~ descriptor~~s is~~ are not released before expiration of the ~~timer~~ time-out period.

19. (currently amended) The method recited in claim 17, wherein the ~~first and second~~ descriptors are written back to a cache memory having a line width of 2N bytes, and the ~~first and second~~ descriptors each have a width of N bytes, where N is a positive integer.

20. (currently amended) The method of claim 19, wherein the ~~first and second~~ descriptors are written back to a cache memory having a line width of ~~32B~~ 32 bytes, and wherein each ~~the first and second descriptors each have~~ descriptor has a width of ~~16B~~ 16 bytes.